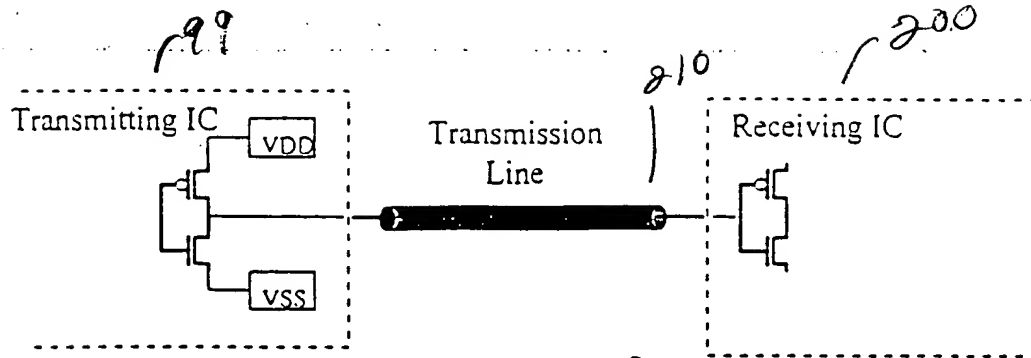


Figure 1 column parallel architecture for focal plane A/D conversion



(a) Fig 2

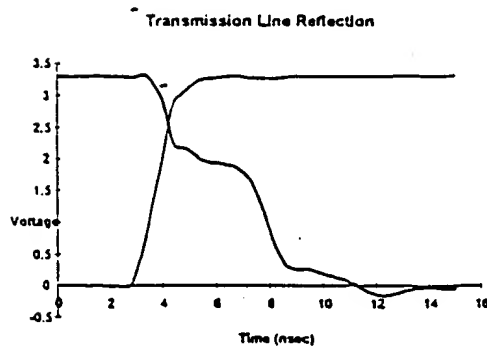
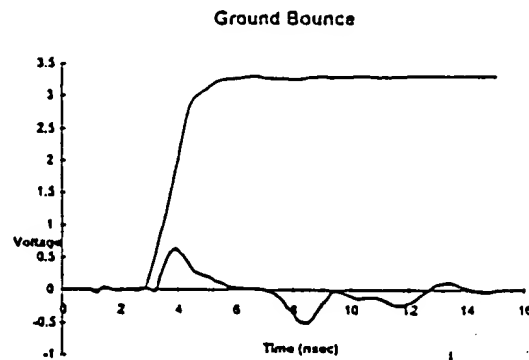


Fig (b) 3a



(c) Fig 3b

Figure 1 (a) Conceptual diagram of standard CMOS I/O. (b) Output waveform when driving 1ft of coax cable. (c) Glitch voltage at the transmitter ground line.

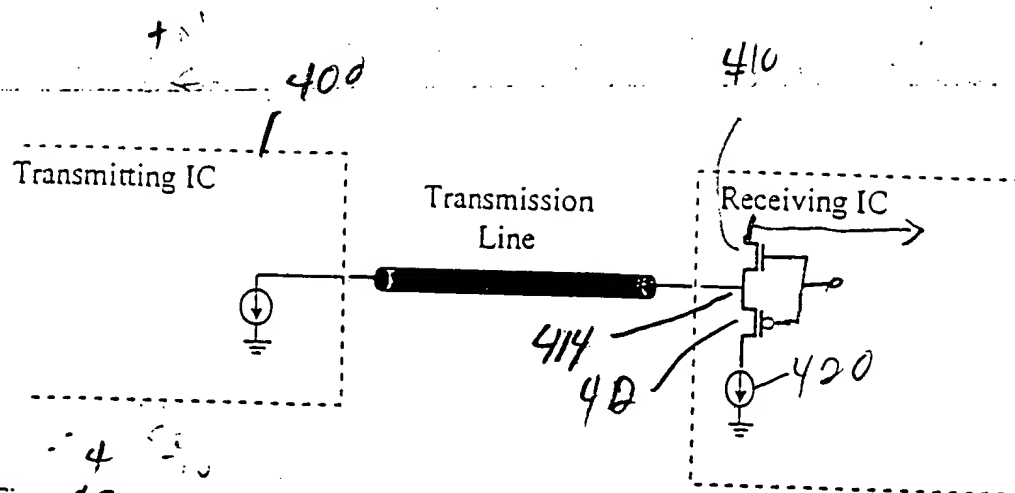
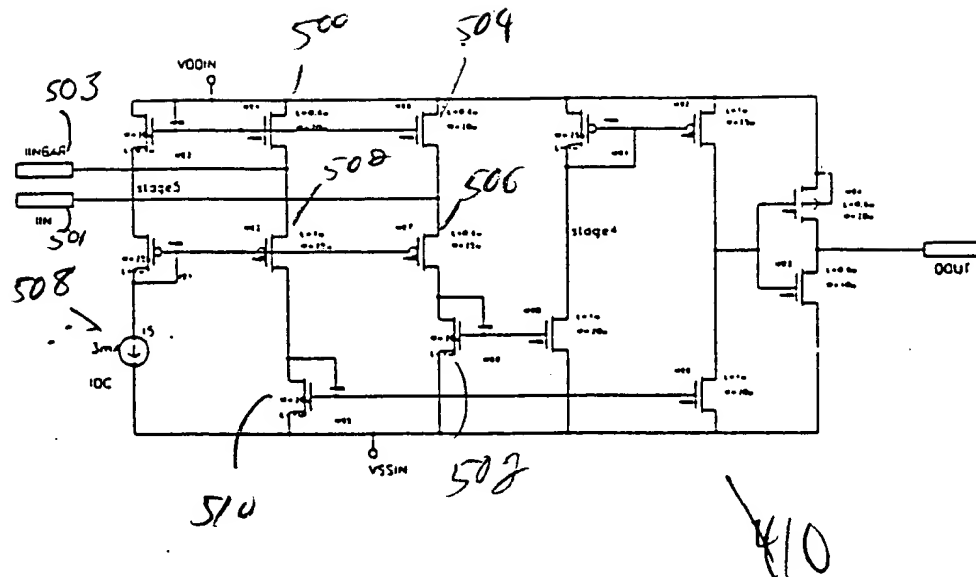


Figure 1 Conceptual sketch of CMOS current mode I/O technique



5
Figure 3 Schematic of receiver circuit.

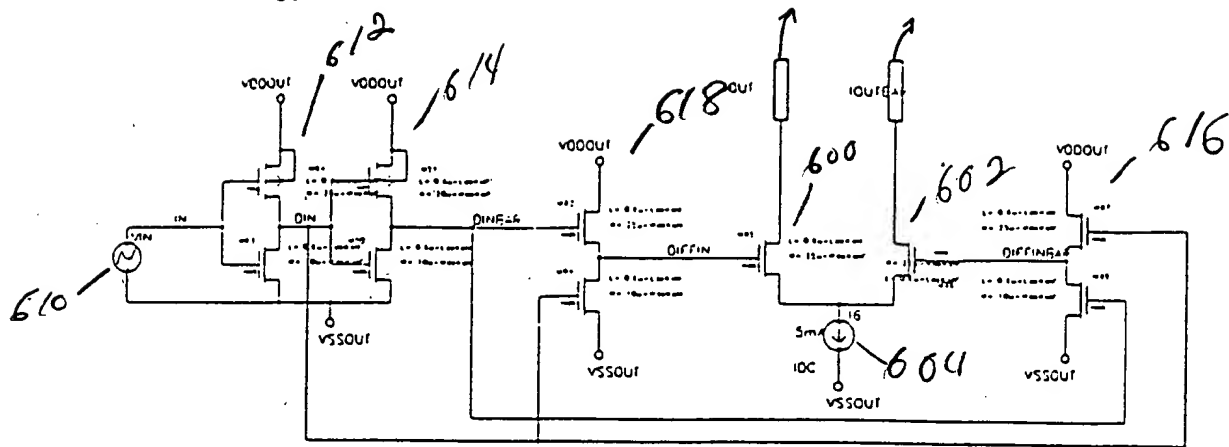


FIG 6

(a)

Output Response at 400 Mbit/sec

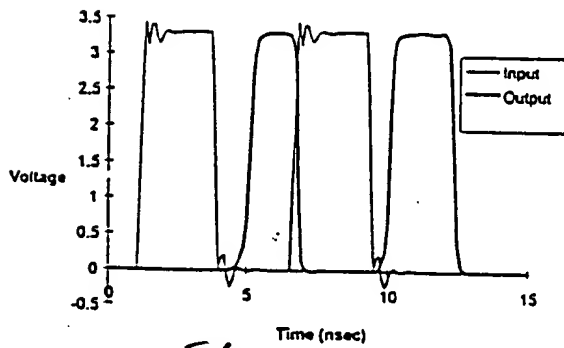


FIG 7a (b)

Ground Bounce

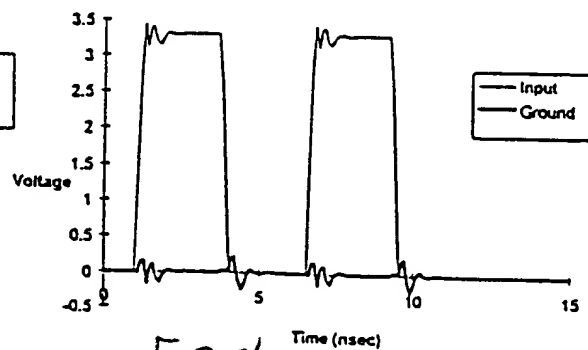


FIG 7b (c)

Figure 14/14 Schematic diagram of 1st output buffer. (b) Output waveform. (c) Glitch voltage at the ground line.

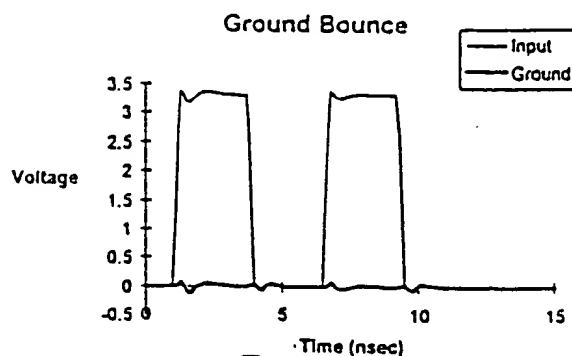
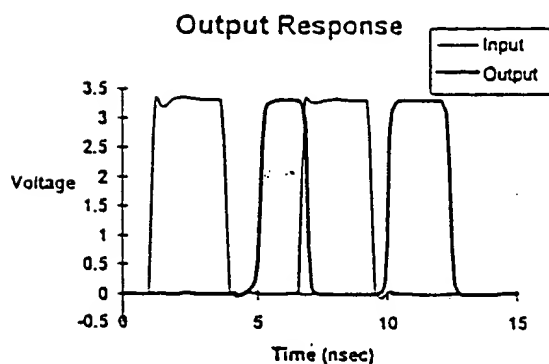
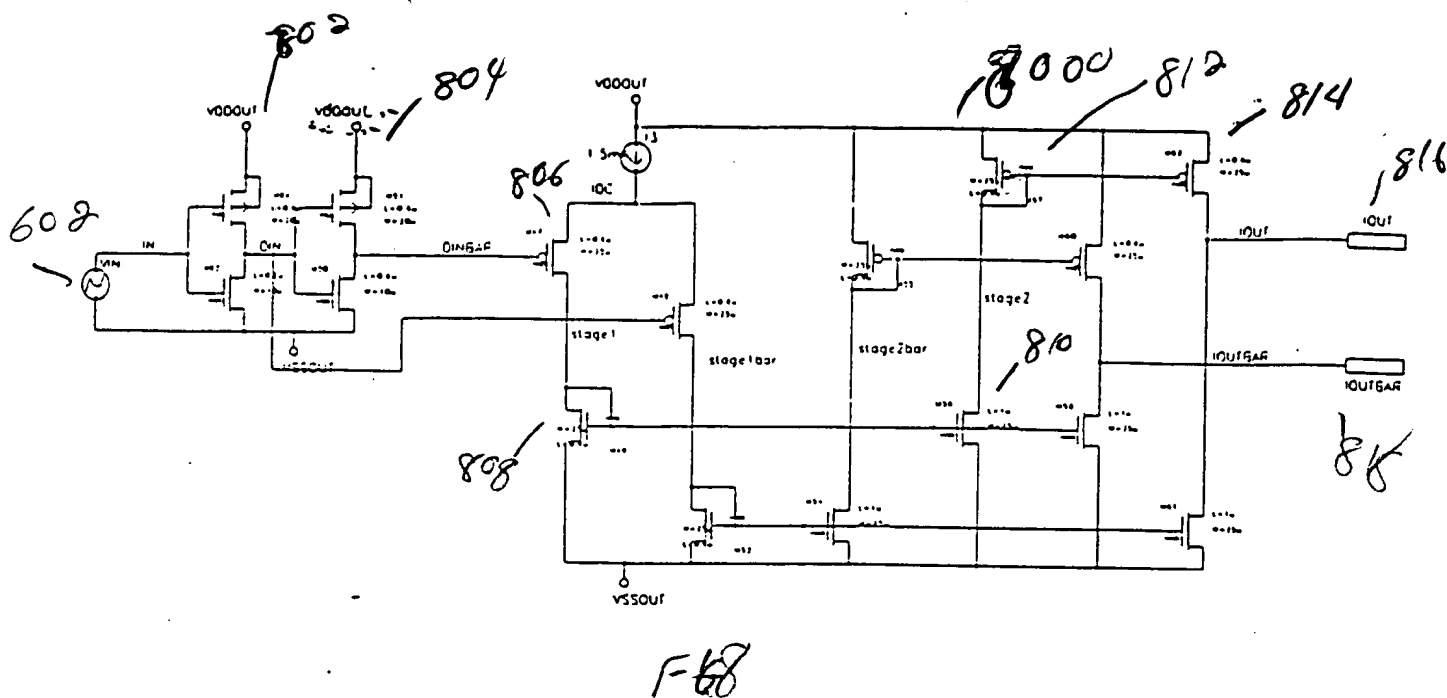


Figure 9(a) Schematic diagram of 2nd output buffer. (b) Output waveform. (c) Glitch voltage at the ground line.